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# Semiconductor Equipment and Materials: Funding the Future

## EXECUTIVE SUMMARY

The semiconductor industry is at a crossroad. The microchip has contributed to remarkable improvements across the electronics sector and produced enormous economic and social benefits. However, without significant attention, the pace of innovation that has led to these unprecedented advancements will be curtailed.

The microelectronics sector has spurred a global information revolution through the persistent drive to make semiconductor devices faster, smaller and cheaper. For 40 years, the catalyst at the heart of this progress has been a relentless pursuit of advances characterized by the famous “Moore’s Law” observation. Historically, these advances have been achieved through innovation realized by research and development (R&D) at the leading edges of physics, chemistry, materials science and other scientific disciplines. Now, a gap is rapidly emerging between the innovation necessary to keep up with “Moore’s Law” and the availability of R&D funding in the semiconductor equipment and materials industry.

In fact, semiconductor manufacturing productivity and the many associated economic benefits of technological progress are threatened by a looming R&D funding gap, which at the current trajectory, could reach upwards of US\$9.3 billion by 2010.

The semiconductor equipment and materials industry will be able to afford a projected annual R&D budget of \$10.4 billion by 2010. However, the estimated R&D funding required for the continued scaling of CMOS technology in accordance with Moore’s Law will reach \$16.2 billion. If the industry proceeds with development of the next wafer substrate size, annual R&D funding requirements will swell to \$19.7 billion by 2010. It is believed that these numbers may well be conservative and, based on possible slower industry growth coupled with slower R&D investment rates and continued heavy pricing pressures, the gap could be even larger.

Among the many challenges in the next decade, three are particularly daunting: new materials and process integration, next generation lithography, and the prospects of a continuing wafer size progression.

Total R&D spending has escalated as technology starts to converge on barriers created by the basic laws of physics. Many of these barriers can be overcome with new structures, processes and materials—but at a cost and in a timeframe that is not feasible from a business management standpoint.

Furthermore, the difficulty is no longer just technological. Traditional R&D affordability is increasingly influenced by changing market dynamics such as commoditization, cost pressure and narrower margins.

The funding gap is further exacerbated by other inefficiencies that could be minimized by a combination of better industry priority setting, pre-competitive partnering, strengthened business models and elimination of redundant or wasteful research.

Also, the industry roadmap does not encompass sufficient business judgment to estimate the probability of success for various solutions and occasionally gets ahead of real industry needs. Unless something changes, the semiconductor equipment and

materials industry will not be able to afford to keep up with Moore's Law.

There are five potential solutions to close the R&D funding gap. They are:

- (1) **Stronger business models to maintain R&D spending in cyclic downturns**
- (2) **Reduction of R&D costs**
- (3) **Sharing or partnering**
- (4) **External funding**
- (5) **Government funding/subsidies**

In reality, it will take a combination of these to ensure the future of this industry, which is vitally important to the global economy. A sixth alternative is to let the pace of progress slow down to meet the affordable funding level.

This white paper is an independent investigation commissioned by SEMI to assess the R&D situation and provide potential direction to mitigate disruption to continued industry advancements.

Input from semiconductor, equipment and materials companies and other industry participants has been obtained to characterize the complex issues and determine the magnitude of the funding shortfall for necessary R&D.

The white paper includes recommendations for semiconductor device manufacturers, equipment and materials suppliers and governments, all of whom have a vested interest in assuring the continued advancements in microelectronics manufacturing technology.

## INTRODUCTION

The semiconductor manufacturing business has in aggregate grown significantly, but experiences major boom-bust cycles. Over the past decade, revenues have continued to grow, but at a much slower rate and with more volatility. Since the 2000 semiconductor sales peak, chip sales have reached a new high, but the equipment and materials supplier base has not regained the prior peak levels, having experienced slower growth rates than their customers. During this period, the semiconductor device industry has substantially increased R&D spending, while the equipment and materials companies have barely managed to maintain flat R&D spending. Ongoing advances in manufacturing productivity and the many other benefits from the continued progress of semiconductor technology are at risk from any such shortfall in R&D funding.

This white paper identifies the major R&D issues facing the semiconductor equipment and materials industry, and how they are currently being addressed. However, it should be noted that technology developments occur rapidly, so schedules and technology directions are always subject to change. It also assesses the gap between the R&D funding required to maintain the progress of Moore's Law and a forecast of what the industry can reasonably be expected to sustain.

The scope of this paper is global, with findings based on research, analysis and surveys conducted with companies from multiple countries with global customers. The methodology used to build the supporting information and arguments included a combination of industry research, financial analysis, and in-depth interviews with 60 executives from 45 companies in Europe, Japan and the U.S.

Detailed results of the industry financial analysis and the surveys are contained in the attached appendices. Unless specifically stated otherwise, all comments apply globally. However, for consistency, all financial numbers are expressed in U.S. dollars.

## MAJOR TECHNOLOGY CHALLENGES

- **Too many new materials and selection/convergence is happening much too slowly**
- **Next Generation Lithography—many questions/ too many options**
- **Materials companies need more effective shared lab resources for integration and testing**

Semiconductor manufacturing comprises many different technology components as described in the ITRS (International Technology Roadmap for Semiconductors) document. Three key technology challenges will loom ahead of all others during the next decade; new materials and process integration, next generation lithography, and wafer size progression. They are primarily centered around wafer manufacturing and will be discussed first, before we examine the various industry segments.

### New Materials and Process Integration

Traditional CMOS transistor structures have been linearly scaled down almost as far as they can go. However, Moore's Law will be extended by changing the structures and by using new materials with different electrical and physical properties. As a result, after several decades with minimal changes to the material set used in device manufacturing, we are seeing the proposed adoption of many new materials for dielectrics, gates, substrates, strain engineering, etc. The most recent technology node introduced into production, 90 nm, included three or four new materials. The next node, 65 nm, will require up to a dozen new materials and beyond that, some experts believe up to 30 more materials may be introduced. This is a significant challenge considering that prior to 2000 the industry only used 16 different elements in semiconductor manufacturing.

Consider, for example, the conversion of gate dielectrics to high- $\kappa$  materials. There are currently more than 10 different materials in evaluation using several different deposition technologies. The number of combinations grows geometrically, driving up R&D expenditures. However, not all of these will be successful. This is an ideal opportunity for pre-competitive research to narrow the choices to a few preferences that suppliers can develop into competitive products. Projects have been initiated at IMEC and International SEMATECH, and these organizations have forged a

link between their respective high- $\kappa$  programs. This collaboration brings together the world's semiconductor manufacturers with the objective of reaching a consensus for these new materials to ensure that proper process equipment for manufacturing is being developed. The success of this project will help the equipment and materials companies minimize redundant and obsolete efforts. More of this type of collaborative effort is needed in other areas.

Process integration costs are increasing even more rapidly. Process complexity is one factor driving this, but others include the new material interactions, and the subtle differences in process sequence between customers. For the toolmakers, any integration that is required within their own tool cluster can be performed in-house at their own facilities. However, this incurs additional cost and work in sourcing blank test wafers from market sources, or from willing customers. This is frequently a challenge.

Materials suppliers often need to purchase process and metrology tools from the OEMs to populate their R&D and applications labs for integration work. Constructing and equipping such a laboratory can cost from \$10 to \$50 million, and further funds are needed to keep it up to date with leading edge tools.

Some process integration does occur at independent consortia such as IMEC, SEMATECH, SELETE, and Albany. However, one key concern here is intellectual property (IP) protection. Another is the issue that these organizations are focused primarily on helping the device makers. Their equipment and materials suppliers have many common interests with their customers, but they also have differences, which are not addressed by the consortia. Even then, not all such third-party research areas have full production-scale process capabilities.

The customer's wafer fab is the best location to perform process integration. Device makers may say they are building the same process technology node, but subtle variations in sequence and specifications can have a large impact on integration results. Despite the need for accurate and timely results, it can frequently be a challenge for equipment and materials suppliers to obtain access to customer facilities. The situation could be improved with better simulation and APC tools to help engineer and optimize processes. The availability of e-diagnostic capability will also enable remote access into the fab from any virtual location and, with automation, will enable global resources to speed up integration.

### Next Generation Lithography

The most expensive line item on the semiconductor capital and R&D budget is photolithography. For a while, all participants were following the ITRS by developing tools, materials and processes using shorter wavelength (157 nm) light. The challenges were substantial, driving heavy R&D spending in the areas of calcium fluoride "glass", photoresists, lenses, steppers/scanners, etc. Then, immersion lithography was proposed. Based on the available 193 nm wavelength of light, the good news was that it obviated the need for 157 nm lithography, calcium fluo-

ride and several other tough technical barriers. The bad news was that several companies had already spent a substantial amount on R&D and preparations for 157 nm manufacturing in what turned out to be a very expensive "blind alley."

The current plan of record through the 45 nm node is to use 193 nm water immersion lithography. Beta tools are currently under evaluation with further development and integration required to reach full-scale production. To go below 45 nm to the 32 nm node will most likely require a liquid other than water, with a higher refractive index, or some other type of next generation lithography.

Beyond immersion, there are three major candidates for next generation lithography—extreme ultra violet (EUV, using 13 nm wavelength light), electron beam direct-write, and nano-imprint. Each approach has its champion, but they all face serious technology and economic challenges. These challenges are not just in the area of equipment and materials, but also in the repetitive costs of the mask tooling required for each new chip design. R&D investments will be extremely high, but not all will yield returns. This would appear to be an area in need of pre-competitive cost/benefit analysis to narrow the choices and align resources to ensure the success of the most likely solution.

### Wafer Size Progression

In the past, leading U.S. chip manufacturers were willing to bear the brunt of the R&D costs necessary for a transition to larger wafer sizes. However, when the industry migrated from 200 mm to 300 mm wafers, the equipment and materials companies carried the R&D burden with the promise of financial returns as the device industry moved to larger wafers for production.

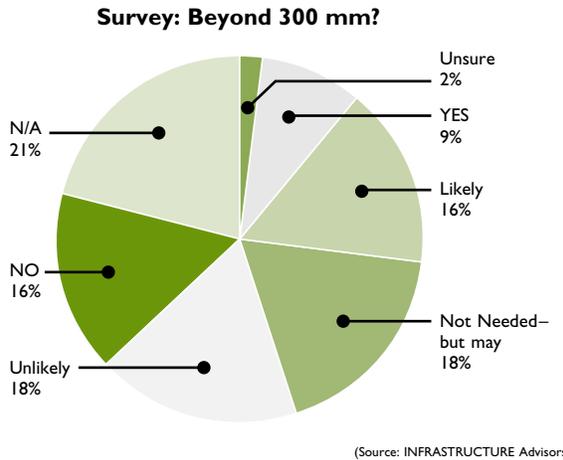
300 mm development work started in earnest in 1996, but delays caused extensive redesigns to meet shifts in the target feature size node. For many companies, 300 mm R&D costs continued through to 2003. Few survey respondents could quantify their specific 300 mm conversion R&D costs. However, we were able to estimate an approximate \$12 billion cost spread over the 1996–2003 timeframe.

The next transition, from 300 mm to a proposed 450 mm diameter wafer, is now being discussed by IDMs. A move to 450 mm wafers will clearly only be possible for a few of the largest device makers, given that a 300 mm fab costs about \$3 billion. Questions that naturally come up are ... "Who will pay for it?" and "What alternatives could deliver the same productivity gains?"

The survey results indicate that 52% of respondents believe it will not be economically viable or necessary to go beyond 300 mm wafers. Despite the obvious return of lower cost per square inch of silicon, there are several other economic barriers that might preclude an effective return on the development investment.

There will be fewer device makers who can afford the transition to the next wafer substrate. These customers will need to fund the investment in a way that not only brings a return to them,

but also to the supply infrastructure whose participation will be required. The real motivation for moving to larger wafers is improved silicon productivity. However, this can be achieved through means other than traditional wafer diameter scaling. Historically wafer size transitions have been driven by technology working groups that set the specifications and define the high-level design criteria. However, the consensus is that economic benefits will likely be less compelling beyond 300 mm and should be thoroughly studied before industry committees are formed to start the detailed technology planning. If 450 mm is to happen, it will take 7–10 years of planning, and the customers pushing for it must be prepared to fund it.



## INDUSTRY SEGMENT FINDINGS

### Equipment Suppliers

- The equipment industry performs little pure research—mostly applied research
- Lithography is the most critical research area, with current optical technologies expected to fail below 45 nm
- Equipment requires a large burden of post-warranty support, to be operated in a win-win environment
- Process complexity within the wafer fab has risen to the point that process integration is becoming an increasing burden
- Cost/performance trade-offs in development are a challenge to “back-end” suppliers
- New wafer fab materials, such as copper and low- $\kappa$ , are impacting packaging

R&D costs for semiconductor equipment vary depending on the tool type, technology challenge and size. There is relatively little pure research performed by the equipment industry; it is mostly applied research for product development. In most cases, equipment products require design skills based on the basic science disciplines such as physics, electronics, optics, mechanics, material science, organic chemistry, inorganic chemistry and soft-

ware. Availability of these skills has led to the geographic clustering of equipment companies in the U.S. (e.g. Silicon Valley), Japan, and Europe. However, these skills are starting to atrophy in those regions due to fewer domestic university graduates being produced to meet industry needs. If this continues, it is likely that the equipment industry, like the device industry, will migrate to other regions such as Asia and India where these skills are being actively developed.

The semiconductor equipment industry, which has traditionally grown at rates in excess of the device industry, now faces long term growth rates equal to or less than their customers. The challenge is that the technology is getting more difficult to implement and R&D costs are increasing. As equipment revenues experience modest growth, the industry has kept investing to the point where many smaller companies are spending as much as 20 percent of revenues on R&D. This is not sustainable over the long term. The biggest issue is not technology. It is that process complexity within the customer’s fabs has risen to the point that process integration is becoming an increasing burden.

### Wafer Fab—“Front-End”—R&D

The wafer processing or front-end equipment suppliers are recognized as providing value to the device manufacturing effort. Their tools and materials help construct the multiple layers of silicon and interconnect wiring that creates the chip’s functionality. Fab equipment R&D costs range from \$5 million to over \$100 million, depending on the tool type and application.

The customer base for equipment suppliers is consolidating and migrating towards Asia. Fewer device makers can afford to invest \$3 billion in a new wafer fab, so the primary customer base for front-end suppliers is shrinking to a just few major IDMs plus the wafer foundries.

The most critical area for research is lithography, where current optical technologies are expected to fail below 45 nm. It is below this level where next generation technologies will be required. The survey found multiple opposing views on whether EUV, E-Beam, or imprint lithography would provide the optimum, cost-effective solution. Each has its own substantial technology hurdles to overcome. More importantly, it needs to be determined if the available market and business models can support a sufficient return on investment for both the suppliers and their customers. The focus today is almost exclusively on the technology challenges, but the industry could benefit from a pre-competitive appraisal of both cost and technology to determine which approach has the highest probability of success.

In other equipment sectors, the challenge is to develop tools that implement the device technology at the defined performance level and with the required productivity to give customers a strong value proposition. Although core competencies vary between equipment segments, the key elements are “systems integration” to provide a complete, functional tool, and “process integration” to make that tool operate seamlessly within the device manufacturing process.

### Assembly/Test—“Back-End”—Suppliers

The “back-end” equipment suppliers have not received much recognition for their contributions towards device value because packaging and test do not enhance device performance and functionality. What they do is assure the quality/reliability and guarantee the performance of devices. They also make it easier for customers to handle and use devices in systems. As a result, the value proposition of the “back-end” is more directed towards end customers using the chips in systems.

Assembly and test suppliers tend to experience more economic challenges in R&D as opposed to pure technology barriers. Technology challenges are generally solvable without a lot of research, but the cost/performance trade-offs in development are more difficult for “back-end” suppliers.

In R&D, front-end suppliers focus on the process, optics, chemistry and device physics. In contrast, back-end suppliers focus on the product and its form, fit and function. Test and handling systems deal with the power, fault detection, and performance of the chips. The test challenge is primarily that of managing electrical performance in the time domain. If a processor operates at 2 GHz, the tester to verify its performance needs to operate several levels ahead of that. With the enormous volumes of test data and high-speed operations, device testers are at or beyond the R&D challenges of super computers.

While technology performance moves forward relentlessly, the pressure for lower priced systems is also relentless. It is becoming increasingly difficult to keep tester technology ahead of the semiconductor devices themselves, so more R&D is required for methods of self-testing high-performance chips—known as BIST, or built-in self-test. This is requiring unprecedented levels of cooperation between designers and test engineers. This move to structural, design-for-test methodologies has led to the introduction of lower-priced test systems. However, device makers still need to purchase a few of the expensive high-performance functional testers for device characterization. The R&D challenge for ATE companies is that these characterization systems are the most expensive to develop, but if customers only buy a few, where is the return on investment?

Test companies have invested a portion of their R&D budgets into creating more extendable system platforms with longer lifetimes. There is also a move afoot to establish an “open architecture,” but so far this has only gained the support of one major ATE vendor and several instrumentation companies. While not exactly creating a “standard” open architecture, this move has encouraged all major ATE vendors to open up their proprietary architectures to some level for third parties to design-in instrumentation.

Semiconductor packaging is also evolving from simplistic mechanical operations to complex processes involving lithography, deposition, etch, etc. to build the package around the chip. Some packages use stacked chips to reach the density levels required for today’s applications. This increased packaging density is requiring wafers to be thinned substantially after leaving the

fab. The package built around the chip is also shrinking to the point where it’s not much larger than the chip itself. End customers such as mobile phone handset and automotive product makers typically drive leading-edge packaging demands. These advanced packaging technologies are requiring suppliers to add new core competencies to their R&D groups that have historically been electro-mechanical in nature. The new R&D skills include disciplines such as chemistry, physics, lasers, thermal control and software.

Although new wafer-level assembly and packaging processes are emerging, the previous generation of wire bond assembly technology is not dead. R&D is still being actively performed to increase the pad-pitch density and productivity of wire bonders. However, this is approaching some technology barriers that may accelerate the migration to wafer level technologies. There are also packaging issues resulting from new materials used in the wafer fab. Bonding to copper, and sawing or packaging soft low- $\kappa$  dielectric materials present challenges that are being addressed in R&D programs. Therefore, the impact of these new fab materials is not constrained to the wafer fab itself, but has far reaching implications through the “back-end” which must be addressed.

From a handling perspective, only a few tools need to touch wafers since they are diced and separated into individual chips (die) at an early stage. Tools that do handle wafers, and therefore require new platforms for wafer size changes, include wafer probers, memory repair systems and sawing/dicing systems. After the individual chips are separated from the wafer format, they are handled either on tape, leadframes or individually. All of these physical form factors require different tool platforms to be developed for each.

### Product Cycle Times

Equipment product development cycles are stretching as technology complexity increases. To compensate, over the last decade almost all system suppliers have adopted smart platform architectures, which span multiple device technology nodes and enable them to bring several products to market based on each platform. The first development of a new platform takes anywhere from two to five years to complete, but on average the development cycle is 2.8 years. This enables subsequent derivative products to be developed and introduced in half that time, typically an average of 1.4 years.

New equipment platforms are generally created to deliver breakthroughs in performance. Platform changes are expensive for customers in that they require extensive integration and testing, meaning they must deliver exceptional performance and productivity improvements to justify the expense. An OEM that brings an excellent new platform to market can open new customer doors and win market share. Conversely, a product that misses the mark will inevitably result in market share losses. Customers typically change suppliers when two things happen: the incumbent fails to be competitive, and a new supplier comes out with a superior product.

Each new product on a platform enjoys a relatively short sales lifespan of three to seven years, with the average being 5.4 years and the volume sales “sweet spot” being in the two to three year range. Platforms typically last for three to five technology nodes—typically 10 to 15 years. Suppliers must not only get the products to market as quickly as possible, they must have sufficient manufacturing capacity to satisfy market demand for successful products. The challenge in the systems business is that volumes are typically low and selling prices high, giving a very granular manufacturing ramp. Small tools are priced at around \$100,000, medium-sized tools are in the \$1 million to \$3 million range, and high-end tools (usually lithography) range from \$10 million to \$20 million and are heading higher with successive technology nodes.

### The Support Commitment

The low-volume, high priced equipment business is very different than high-volume device manufacturing. In the equipment business, once a product is shipped it requires ongoing support and upgrades. The same is not true for semiconductor devices, which are generally manufactured, shipped and forgotten about, while the manufacturer moves on to the next new product. Survey respondents describe customer expectations for active equipment support to be in the 10 to 15-year range, with the real desire being “infinite.” This is a significant challenge for the equipment industry. Many equipment companies offer service programs where, for annual maintenance fees, they will support the product well beyond the original warranty and to subsequent owners. A major challenge arises in the burgeoning Asian semiconductor manufacturing market where the expectation is to not have to pay for support beyond the purchase price.

Some of the challenges in supporting products beyond the initial 5 to 10-year lifetime include the fact that component suppliers often obsolete parts used by the OEM to build the tools. These can be controllers, computers, etc. that have short silicon-based lifecycles. This is most significant in systems that have high semiconductor content such as ATE. The semiconductor suppliers phasing out these components are often the same companies that are buying the equipment and expecting extended support for their tools. Faced with component obsolescence, equipment OEMs may have to consider a redesign of the system module using new components. This is an expensive proposition not only in terms of ROI, but also because of the lost opportunity in having R&D staff perform a mundane redesign rather than develop a new product with strong market potential.

Some OEMs deal with this by offering trade-in programs to entice customers to upgrade to newer systems. Others buy back old systems and cannibalize them for the obsolete components to keep the remaining installed base alive and well. Some OEMs sell off old product lines to after-market suppliers to achieve a graceful exit in the eyes of the customers. Supporting a product during the warranty period is a part of doing business, but supporting it beyond the warranty period for an extended lifetime across multiple owners must be managed profitably by the OEM in a win-win relationship with the tool's owner.

### Sub-System Suppliers

- **There is tremendous price/cost pressure on sub-system suppliers**
- **Cost is designed-in, but customers demand price reduction with no redesign permitted**
- **NRE funding may return to help manage the risk/reward**

Sub-system suppliers manufacture modules such as power supplies, gas flow controllers, laser sources, RF generators, robotics and automation interfaces that are incorporated into capital equipment. They often sell directly to device makers that need the technology to integrate the OEM's tools into their device manufacturing operations.

Sub-system suppliers share many of the same business issues as equipment OEMs, but face some additional challenges. They have to service two discrete customer bases; the OEMs that incorporate their modules into tools, and device manufacturers that buy their modules directly for special features and replacement value. This is clearly a challenge as reflected in the financial business model analysis in the appendix.

OEMs that outsource to sub-system makers are good, but demanding customers. They rely on the sub-systems suppliers to reduce cost when the device manufacturers and market forces pressure them to reduce tool prices. It's not unusual for OEMs to ask these suppliers for a 10 percent to 20 percent price reduction in a relatively short order. Most of the manufacturing cost is set by design. Other than taking it out of profitability or in turn squeezing their supplier base, the only smart way for sub-systems companies to reduce their cost is through re-design to take advantage of new technologies or innovation. The challenge here is that OEMs and device makers are extremely reluctant to accept change once a tool is qualified. In fact, under any type of “copy exact” program, change is specifically not allowed.

When a module is designed into an OEM's tool, it locks a particular sub-system supplier to that business. The opportunity for competitors to get back into that OEM is when the next tool is being designed. During interviews for this report, it was apparent that there are a few good examples of partnering between OEMs and sub-system suppliers, but it was also clear that many such partnerships are little more than “lip service.” These relationships are frequently strained when design-in decisions are being made and when OEMs return for further price reductions beyond the original contract.

In the 1980s, it was common for OEMs to essentially “hire” sub-component suppliers to design a module for them. They would pay non-recurring engineering (NRE) fees to have that module designed to their requirements. As the sub-systems companies became stronger, a competitive tactic was to waive the NRE charge for a commitment to the business and pricing levels that would give a return to the sub-system supplier over time. This entrepreneurial approach shifted risk onto the shoulders of the sub-system community with design resources being gambled as investments to secure design-win returns. OEMs are now

pressuring sub-systems companies for pricing levels based on pure manufacturing cost, without taking into consideration the amortized design/development costs that went into the products. This is not a sustainable situation, and the sub-system industry may in future seek the return of NRE payments to fund the riskier custom development programs.

### Materials Suppliers

- **The semiconductor industry's unique material requirements drive a heavy R&D commitment with virtually no leverage to other industries**
- **New materials have very long adoption cycles and a slow ROI on invested R&D**
- **Pricing materials to value will strengthen margins and enable more investment in R&D**
- **Materials companies need more effective shared lab resources for integration and testing**

The materials industry is faced with the challenge of Moore's Law, which drives continuous increases in silicon efficiency. By definition, if silicon efficiency increases, it takes fewer materials to make more chips. This is why the materials industry has not grown as fast as device industry revenues. While the materials used in device manufacturing remained largely unchanged up until 2000, they were viewed as commodities and suffered heavy price and gross margin pressures. Since 2000, the industry has been aggressively adding new materials to support the continuation of Moore's Law. While these materials are used in relatively small volumes, they add substantial value to device manufacturing. Although some of the new materials may have better margins than the legacy materials used by the industry, their volumes have not been sufficient to offset the significant margin erosion of the legacy materials resulting in a continuing decline in profitability for materials suppliers over the last five years.

Large materials companies find that the R&D required to support the technically-demanding semiconductor device industry is substantially higher than that required for other industries with larger markets offering higher returns. In addition, materials used by the semiconductor industry have little, if any, application outside this particular industry. As a result, there is little R&D leverage beyond the semiconductor industry and unless the suppliers are committed to the industry as a stand-alone market, they will be drawn to other markets for better ROI. Over the last few years, companies such as Kodak and Ashland Chemical have withdrawn from the semiconductor materials market. There continues to be concern that other chemical industry "giants," viewing the high risk/small market, will also exit over time.

There is a growing sentiment that materials should be priced not based on their manufacturing cost and volumes, but on the value they contribute. Materials technology is highly specialized, requiring substantial R&D to develop not only the chemical composition of the product, but also the manufacturing process and formulation. This is the intellectual property (IP) that the materials suppliers bring to the table.

The challenge is that while product R&D times are relatively short, the integration into the customers' process takes a long time. Survey respondents indicate that typical development cycles for evolutionary products are on average 3.5 years, compared with 2.8 years for the equipment companies. However, due to lengthy adoption cycles for new materials, returns on the original R&D investment can take more than five years. For revolutionary new materials such as low- $\kappa$  and new photoresists, it can take anywhere from nine to 15 years from first development to market acceptance and commercial production. The R&D cost for this can range from \$50 million to \$150 million.

More than 30 new materials are being considered for introduction to device manufacturing over the next several years, severely challenging the resource bandwidth of materials companies. In the dielectric area, many new low- $\kappa$  and high- $\kappa$  materials are being proposed, requiring substantial parallel efforts to develop and evaluate/integrate each of these with equipment makers and device makers. Many of these approaches will end up being redundant, widening the risk-reward ratio for the materials companies. Any effort to quickly narrow the material selections will help the materials companies maximize their R&D investments.

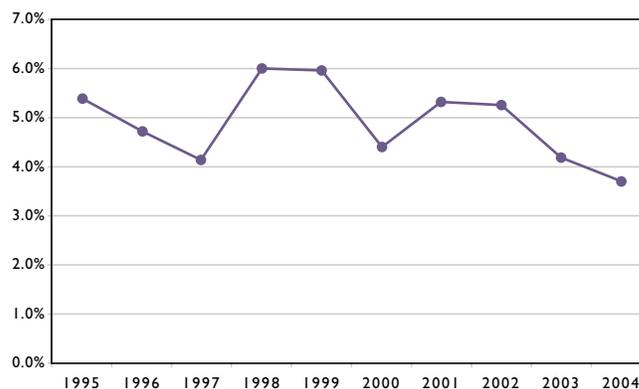
Integration is a major challenge and requires close cooperation between materials companies, equipment suppliers and device makers. This three-way cooperation can often present challenges, particularly in the area of IP conflict. Recently, there have been more examples of equipment suppliers developing materials in the low- $\kappa$  arena and claiming their own material IP rights. This can lead to a strained relationship between materials and equipment suppliers.

As mentioned previously, materials companies require access to working equipment to run experiments on new materials. Shared labs would help reduce cost, but need to be managed independently and should ideally be located in close proximity to centers of R&D excellence.

### Wafer Suppliers

Silicon wafer suppliers represent the largest single materials market in the chip industry. They face some of the previously mentioned challenges, but have some unique ones of their own.

**Wafer Supplier R&D as Percent of Revenues**



(Sources: SMG, SEMI)

Wafer manufacturers have traditionally spent an average of 5% of revenues a year on R&D, with the trend in 2003 and 2004 falling to the 4% level (see chart). This R&D investment is much lower than other industry segments, indicating that R&D spending is not a major issue faced by wafer suppliers. Instead, the real challenge is the long delay experienced from the time of larger wafer diameter R&D investments to the point where consumption begins for those new wafers. The other factor is the large capital investment required to ramp wafer manufacturing capacity—almost as large as the investment made by device makers in their fab capacity. The capital investment in wafer-making plant and equipment is substantial and with slim gross margins, it typically takes some time to recoup the original investment. Annual capital investments for the group are typically in the range of 15% of revenues, but when wafer transitions occur, this can double for a period of two to three years. The wafer manufacturing industry has consolidated substantially over the last several years, so we would assume they can attain reasonable pricing and margins to support their R&D objectives.

## MANAGING R&D

- ITRS—only used by equipment and materials companies for general guidance
- ITRS—would benefit from business as well as technology risk/reward assessment
- University research is used minimally and mainly in very focused areas
- IMEC model is excellent (“research for hire” with a highly-skilled talent pool and IP protection)
- Need to avoid “blind alleys”—more effort required up-front for risk management
- Aggressive technology progression is not necessarily synonymous with creativity

Managing R&D effectively involves identifying the right products and projects to meet customer needs, then undertaking a detailed risk/reward and ROI analysis. The resulting strategy must be implemented flawlessly under constant management supervision and review. External resources are available, but the key factors are to make the right decisions and execute them quickly.

## ITRS and the Company Roadmaps

Most equipment and materials companies indicated that they use the ITRS only for general guidance, while sub-system suppliers felt they had little use for it. The general view is that the ITRS is of more direct use for device makers than equipment and materials suppliers. Many expressed a concern that the ITRS, while it may be useful from a technology perspective, did not encompass sufficient business judgment to estimate the probability of success for various solutions. As a result, the roadmap has the potential to drive too many parallel, redundant and costly R&D efforts. Examples cited include wafer diameter

increases beyond 300 mm, mask/reticle costs, etc. The only direct economic metric in the 2004 ITRS is for packaging cost.

The view was also expressed that the ITRS occasionally gets ahead of real needs. An example cited was the low- $\kappa$  dielectric program, which was too aggressive and suffered a five-year delay from the original plan. This included substantial redundant efforts on multiple materials causing wasted R&D costs.

In developing and managing their own product roadmaps, suppliers spend a lot of time directly with customers to determine their needs. Several respondents said their most valuable asset in eliciting customer requirements was the applications team, which is typically hands-on with customers. Frequent high-level technology roadmap and business reviews are also a critical part of aligning customers with suppliers. For smaller suppliers, this frequent, high-level customer access is often more of a challenge. Larger companies tend to have stronger relationships with customers and easier access to make “partnering” more effective.

## Universities

University research is being used selectively and in a relatively small way by the equipment and materials industry. Most projects are focused on either specific pure research or on specialty analysis and metrology to help troubleshoot particular problems.

Most activities at universities are based on strong personal alumni relationships with the academic staff. Many of these are located relatively local to the company and have a technology specialty that is aligned with company needs. Specific university funding data was not available from companies, but most responded that they typically contribute less than \$50,000 per annum, and a few have occasionally donated equipment to universities.

One of the biggest challenges is IP. More universities now see IP as a way to boost funds through licenses and royalties, and are becoming aggressive about IP ownership. As a result, some companies that have competitive needs to own the IP are using universities only for very early pure research. This gives companies more time to evolve the early research results into their own proprietary IP that can be commercialized. By aggressively seeking income from IP, the universities are raising barriers to collaborative work with industry.

## Consortia, etc.

There are many consortia around the globe and they each take different forms. The classic consortia are those such as International SEMATECH, SELETE, Medea, ASET, IMEC, Albany Nanotech, etc. There are others like APiA and SECAP, the advanced packaging initiatives, that are often referred to as consortia, but do not strictly fit that definition. The “alliance” definition is a better description since these organizations have built collaborative relationships to commercialize their products and membership is fiercely competitive—companies are either in one or the other and not both. SECAP has recently disbanded, having “completed its mission”.

True consortia are more open in membership with clear pre-competitive objectives to help address common industry technology barriers. For example, SEMATECH was originally set up to strengthen the U.S. semiconductor industry, then evolved over the years to its international role of today. In Japan, there are many more consortia of varying sizes. For example, ASET is focused on advanced technology research while SELETE's focus is on the nearer-term challenges in developing technologies for production. ASET is conducting pre-competitive research into such critical areas as next generation lithography technologies, while SELETE, like SEMATECH in the U.S., played valuable roles in the development of 300 mm wafer manufacturing technology.

IMEC is often referred to as a consortium, but is really an organization offering "research for hire." In all of the survey interviews, IMEC received the most praise from the equipment and materials companies for its technology, focus, IP protection and results. IMEC is seen as having the ability to openly share the results of experiments with partners, and to strongly protect IP while doing so. Unlike consortia, IMEC is not a consensus-based organization, which gives it the ability to be less political and more focused.

IMEC is funded by various direct and indirect government sources to levels of approximately 25 percent of the total operating budget, with the majority of funding coming from industry sources in the form of membership fees and project funding. IMEC also receives indirect funding in the form of assignee staff (approximately 400 out of 1,300 total staff) and substantial discounts on capital equipment. The IMEC staff manages the operation like a business, with tight controls on project management and IP protection.

Most consortia are focused on developing solutions to semiconductor manufacturing problems, but IMEC also appears more receptive to including equipment and material companies as partners. There are lessons to be learned from the IMEC model that could be applied to other consortia around the world.

## “**Blind Alleys**”

In a complex technology such as semiconductor manufacturing, there is potential to be led down “blind alleys” that incur substantial R&D investment but do not yield returns.

One example is 157 nm lithography, which was shut down in favor of 193 nm immersion lithography. Several equipment, materials and sub-system suppliers invested hundreds of millions of dollars in R&D for 157 nm technology before the “plug was pulled,” and resources switched to 193 nm immersion. It is high-stakes gambling for suppliers to pick one potential alternative and run with it through development to gain a competitive edge. A more conservative approach would be to invest some collaborative pre-competitive resources to assess the most feasible and likely solution and then apply any competitive advantage to develop winning products.

Another example of a “blind alley” is Rambus DRAM memory

test, which was driven so hard that four large equipment firms each spent an estimated average of \$40 to \$50 million on R&D for purpose-built testers, only to find that market forces relegated Rambus DRAMs to a niche and the demand for these expensive systems disappeared. A small portion of R&D has benefited other projects, but essentially only one supplier remains in the semiconductor memory test business.

Equipment and materials companies need to focus R&D spending on developing the right solutions to minimize wasted resources. However, in the highly competitive semiconductor market, pre-competitive research co-operation doesn't occur very often. IMEC is one of the few independent research centers undertaking this type of activity.

One of the best ways to validate a technology is to have the customer fund some of the research and/or make commitments to purchase the end product. This was more prevalent in the 1980s, but has been infrequent since. If the device maker stands to gain most from a given technology and is making substantial commitments to it, funding key strategic partners is a worthy consideration. The only examples found of this approach were among small and medium-sized companies where the suppliers had the technology, but did not necessarily have the means to fund the project on speculation.

## Thinking “**Out-of-the-Box**”

Although the semiconductor industry is very aggressive about pursuing the technology to implement Moore's Law, it seldom draws breath to look for creative, “out-of-the-box” solutions to problems.

For example, barely have 300 mm wafers been implemented, and top semiconductor technologists are asking “what's next?” Is it 450 mm as some would propose? Let's think about why larger wafer sizes have been adopted over the years. The main reason has been to increase the scale of silicon productivity. At the 300 mm diameter, we certainly have economies of scale, but we also have driven the cost of owning, operating and filling a wafer fab to the point where few can afford it. Moving to 450 mm diameter wafers will only aggravate this problem.

Few are looking for alternative ways to dramatically improve silicon productivity. Take, for example, today's state-of-the-art wafer fab running processes with more than 30 masking steps and taking over six weeks to process wafers. If one wafer were to be processed on its own with no delays through the fab, it would take less than 10 percent of that time. Wafers are processed in fab lots of 25, with substantial “wait” times slowing the productivity. Maybe this should be studied as an area to increase silicon productivity and capital utilization.

Another thought is that when 300 mm fabs were planned, it was anticipated that some “mini-fabs” would be built for device makers that did not need the huge output potential of a full-sized fab. In reality, we have not seen these mini-fabs come on-line. The way that fab construction is performed today, it is not economically viable to build and operate a mini-fab. A question to address would be: “How can we build small, flexible, modular

300 mm mini-fabs that operate profitably?"

In the U.S., Europe and Japan the semiconductor, equipment and materials industry population is aging, with many of its veterans heading off to retirement. The entire industry is based on the basic science disciplines of physics and chemistry, which have been largely ignored by high schools and colleges in favor of social, business and arts programs. As a result, there is a shortage of qualified, bright young graduates to challenge conventional wisdom and stimulate innovation. This problem does not appear to occur in Asia where physics, chemistry and engineering careers are encouraged and graduates are produced to meet the needs of their growing industries. The U.S., Europe and Japan should actively promote science and engineering education to replace the resources that created these industries and maintain the necessary technology expertise.

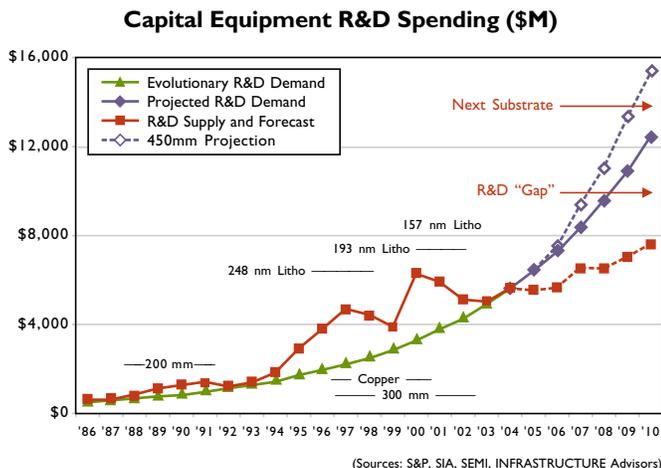
Complacency has led the industry to believe that aggressive technology progression is synonymous with creativity. However, there appears to be plenty of room for more "out-of-the-box" thinking.

### THE R&D FUNDING GAP

- To support the device industry's objectives as defined in the ITRS, the equipment and materials industry will need a projected annual R&D budget of \$19.7 billion by 2010
- It is projected that these industries will only be able to fund \$10.4 billion, leaving a \$9.3 billion gap, a number which may even be conservative by some estimates

### Equipment R&D Analysis

Drawing from the data in the Appendices, it is possible to estimate the actual global R&D spending on equipment products. This is shown in the following figure by the solid red line with square data points. From there, a forecast was made of the available spending to the industry and is shown by the dotted red line. This forecast was based on a consensus of equipment industry revenue forecasts through 2008 and thereafter at a long-term industry growth rate of 8%, which is slowing as the industry matures. This market revenue forecast was then used with a 14% R&D spending assumption (see Appendix II) to project the



supply of available R&D funds.

There were several approaches taken to assess the raw demand for R&D funding. These included analyzing historical capital spending patterns, assessing major technology roadmap items, creating a bottoms-up tool development model, and applying the survey results on tool development costs and trends. The result is the blue line with solid diamond data points, which projects the R&D funding demand from 2005 onwards. This does not include any projection for the R&D costs to develop new platforms in support of any next wafer substrate size increment. The dotted blue line does show an incremental projection for such a substrate change, which is in the formative discussion stages within the ITRS. The difference between either of these (blue line) demand scenarios and the projected available (red line) is the equipment funding gap. Even with no increment for next wafer size, the equipment industry is looking at a potential \$4.8 billion gap in attempting to meet a \$12.4 billion R&D demand by the year 2010. If the move to next-generation wafer substrate proceeds per the current ITRS, then this gap will increase to \$7.8 billion.

It is interesting to project the demand line backwards (green line with triangle data points), and see that this exponential line fits with the historic data in the '80s and early '90s. This would appear to be the "evolutionary" spending baseline to maintain the Moore's Law scaling of CMOS technology. Where the actual spending deviates upwards from this, it can be explained by major technology developments such as the DUV lithography nodes, wafer size transitions, copper interconnect, etc. Some of these have been added to the chart to show the development timeframes. The 300 mm transition was clearly a huge investment, which we estimate cost the industry upwards of \$12 billion to implement. By comparison, it can be seen that the 200 mm transition was much less costly to the industry, but bear in mind that IBM funded much of this development, in the same way that Intel funded much of the 150 mm transition.

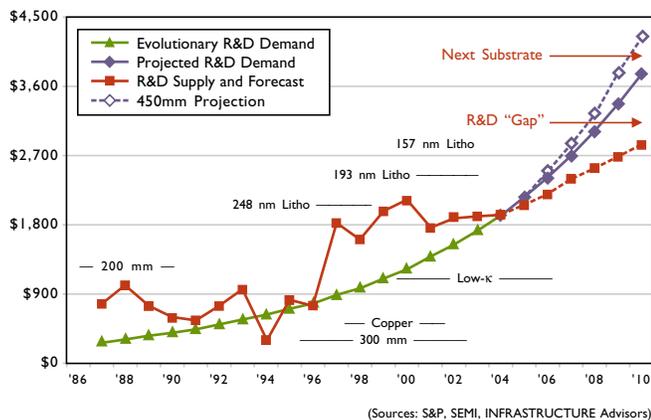
### Materials R&D Analysis

Drawing from the data in the previous sections, with a similar analysis, it is possible to project the supply and demand for R&D funding in the materials segment.

This analysis shows a smaller, but still significant, materials R&D spending gap of some \$930 million by 2010. However, this could climb to \$1.4 billion if the next substrate size needs to be developed in the timeframe identified by the ITRS.

The development of DUV photoresists, 300 mm wafers and copper interconnect all had a clear impact on materials R&D spending in the late 1990s and early 2000 years. The development of 157 nm lithography required not only some early work on photoresists, but also the development of calcium fluoride "glass" for reticles (masks) and lenses since conventional glasses would not transmit the light at a wavelength of 157 nm. In 2004, when the industry switched to 193 nm immersion lithography as the optical solution down to 45 nm, the 157 nm

### Materials R&D Spending (\$M)



R&D was discarded.

Going forward, in addition to the next wafer substrate, there will be major dielectric programs to be funded, including the development of various levels of low- $\kappa$  dielectric materials. The technical challenges associated with introducing this into high-yield manufacturing have been substantial to date. In fact, as documented by the various ITRS roadmaps, low- $\kappa$  technologies have been substantially pushed out until some of these issues can be resolved. As a result, R&D spending on low- $\kappa$  will extend for some years to come, and successive generations will be developed to further reduce the “ $\kappa$ ” value. Currently, there are 15 to 20 manufacturers working on different approaches. Clearly, many will not get a return on their investment. The other dielectric program, for high- $\kappa$  materials, also has multiple vendors pursuing multiple approaches. Unless the choices are narrowed for these programs soon, R&D redundancy and waste will continue.

#### Disclaimer

These gap projections are based on the stated assumptions for future industry growth rates at around 7% to 8% and an equipment R&D spending level of around 14% of revenues. Recent history would indicate that the industry is indeed maturing and experiencing slower growth rates. Slower growth rates will also imply lower R&D spending rates. So, both of these assumptions may well be optimistic, and any drop from those levels would result in the formation of a substantially larger gap.

### The Funding Challenge—Closing the Gap

- Delivering value and pricing accordingly could strengthen business models for stronger R&D funding
- Economic (ROI) analysis should be used up-front to validate major technology directions and avoid wasted R&D efforts—e.g. the next generation lithography technology, and 450 mm wafer transition
- More pre-competitive partnering could be used selectively to share R&D costs
- Customer co-funding can strengthen commitment and

share long-term risks

- Government seed funding could help the equipment and materials industry on key pre-competitive technology challenges

The semiconductor equipment and materials industry will be able to afford a projected annual R&D budget of \$10.4 billion by 2010. However, by that time the demand for R&D will reach an estimated \$16.2 billion in order to continue scaling CMOS technology in accordance with Moore’s Law. If the industry decides to proceed with development of the next wafer substrate size, this will drive that demand up to an annual \$19.7 billion budget by 2010. This implies an annual funding gap of \$9.3 billion by 2010. Unless something changes, the semiconductor equipment and materials industry will not be able to afford to keep up with Moore’s Law.

There are five potential solutions to close the R&D funding gap. They are: (1) higher pricing and gross margins; (2) reduction of R&D costs; (3) sharing or partnering; (4) external funding; and (5) government funding/subsidies. In reality, it will take a combination of these to ensure the future of this industry, which is vitally important to the global economy. A sixth alternative is to let the pace of progress slow down to meet the affordable funding level.

#### Strengthening Business Models

The equipment and materials industry has witnessed rapid change over the last five years, with continued heavy cyclicity, but much slower long-term growth rates. The 10-year rolling CAGRs have dropped from historical levels of around 20% to the 7% to 10% range in the last three years. As shown in Appendix II, profitability has been negatively impacted and R&D investments limited by availability of funding under current business models. In “elastic” markets, reducing the price can increase demand and grow the market, but this is not the case for the capital equipment and materials markets, which are limited by the semiconductor industry.

Therefore, business models must be strengthened. This approach has been successfully applied by semiconductor device makers as shown in Appendix II. They have strengthened gross margins and diverted the funds to support heavier R&D investments. This same approach should be adopted by the equipment, sub-system and materials suppliers. The larger companies, with their broader product portfolios and stronger global infrastructures, are in a better position to succeed in this strategy.

Like the semiconductor device market, the equipment, sub-system and materials segments are populated by fiercely competitive companies. The competitive battles at each customer account are usually centered on technology and performance “shoot-outs,” but customers always pit suppliers against each other for price pressure leverage. The supplier lagging in the technical shoot-out frequently cuts pricing in an attempt to win the business or damage the competitor’s gross margin. The end result is a reduction in the size of the market, which impairs the

industry's ability to fund its future.

The segment that is currently suffering most in terms of weak business models is the sub-system group, which is further down the supply chain and is the recipient of equipment OEM outsourcing. These OEMs need to recognize that sub-system companies also have a heavy R&D burden to be financed, either through funded non-recurring engineering charges or through sufficient gross margin on volume sales. This same argument applies to the OEM—device maker relationship where any customer-specific developments should be funded by NRE from the customer.

Better skills training for suppliers in the area of value selling would improve the situation. Products that have superior technical performance and productivity should command pricing that allows both the customer and the supplier to enjoy returns on investment in a win-win environment. In addition, customer purchasing organizations should be rewarded based on long-term supplier performance instead of short-term cost savings.

### R&D Efficiency Improvements

As previously discussed, the two biggest challenges with R&D are picking the right projects, and having the ability to execute them flawlessly.

Most of the companies surveyed have made tremendous progress over the past decade in improving their processes for selecting projects and managing their implementation. The general approach is to have a marketing-led multidisciplinary team review the feasibility and probable ROI of proposed R&D projects. Once approved, monthly or quarterly project reviews continually validate the market requirements and the progress of the development activity. There will always be room for continuous improvement, but generally speaking, this does not appear to be an area of opportunity for substantial efficiency gains.

The most significant lack of efficiency was found at the higher level where the customer base, via the ITRS roadmap, drove the industry aggressively down “blind alleys.” Examples include the first false start on the 300 mm wafer transition, 157 nm lithography, Rambus DRAM test, and the initial low- $\kappa$  dielectric materials. The ITRS document, undoubtedly an outstanding technology roadmap, could be substantially improved if focused teams were assigned to assess the combined business and technology risks/rewards of major roadmap items. These teams would comprise multi-company, multi-disciplinary experts working in a pre-competitive environment to make the right decisions as early as possible. To date, there have been few pre-competitive activities in the highly competitive equipment and materials market. However, when chartered and staffed correctly, these teams could prevent the industry from venturing down these expensive “blind alleys.”

The next generation of wafer substrate is an issue looming on the horizon, and it has the potential to generate considerable inefficiency in R&D spending. There is need for a real cost/benefit analysis to be performed on the options of proceeding to the next wafer diameter (450mm), versus other options to

increase productivity.

Similarly, the next generation of lithography beyond 193 nm optical immersion has yet to be narrowed down to a single optimal choice. A similar cost/benefit analysis needs to be performed to evaluate the various options and their financial impact from design through manufacturing—before more global R&D funds are wasted.

### Partnering

There have been some interesting and successful cases of partnering to leverage joint R&D towards mutual projects. These have always included companies that have no direct competitive positions in their respective markets. For example, etch suppliers will cooperate with deposition suppliers and materials suppliers, but never with other etch suppliers. The tool OEMs are generally considered “vertical” suppliers, focusing on specific technology and applications. They do partner with some of the “horizontal” suppliers such as those in automation and metrology applications that transcend across all vertical markets.

If the industry can pull some of these players together in truly pre-competitive environments, there may be incentives for other competitors to join together in partnerships. For example, in the materials field, it is becoming increasingly expensive for materials companies to invest in setting up their own R&D labs for test and integration. These expensive resources are seldom fully utilized, so there is opportunity for sharing, and hence cost saving, if an independent body can build and manage such labs in locations where they can be utilized by the global materials industry. Similar examples can no doubt be found in the equipment industry.

### External (Customer) Funding

If a particular piece of research or technology offers tremendous leverage, a company should be willing to invest in it. In the late 1980s, up to the 200 mm transition, there were many examples of large companies such as IBM and Intel investing in equipment and materials companies to develop specific technology. During the 1990s and until recently, the practice of funded development (or non-recurring engineering charges) has dropped back to much lower levels, largely because many of the suppliers raised equity and used it to lower the barriers to obtaining new business. The intent was to leverage the development over the life of the product and avoid the contractual market restrictions associated with funded developments.

Recently, there have been more examples of funded research to solve specific problems. Where a customer potentially has substantial leverage from a technology or product, it makes sense to invest some up-front funding in suppliers to help with their R&D costs. Creative ways to implement this range from simple non-recurring engineering charges to up-front cash deposits for volume order commitments. If a customer invests cash up-front, he is placing “skin in the game” and showing serious commitment to the project.

An important point to consider is that collaborative funding of suppliers can result in substantially increased leverage on R&D

dollars spent. Device maker customers should look carefully at their internal process R&D and consider outsourcing some of it to suppliers, where there is more leverage over a wider customer base. It is often the case that customers each work separately on a common process development problem, resulting in redundant efforts across the industry. If these common issues were identified as pre-competitive, they could be more efficiently funded through the supplier base for solutions. Good examples for this approach exist today in the areas of low- $\kappa$  and high- $\kappa$  dielectric development and integration.

### Government Support

The semiconductor industry has essentially been living off basic research from 30 to 40 years ago. In the U.S., some major organizations such as Bell Labs and IBM have been significant contributors to basic research, but this has been slowing and needs to be proactively supplemented. There are several areas around the globe where governments support the industry through universities, research labs and consortia. These are best leveraged where government money is used to “seed” the pre-competitive stage of a new technology in conjunction with industry investments that are focused on delivering the intended competitiveness and resulting commercial returns.

The challenge for consortia is that they are “managed by committee,” tending to make them more bureaucratic and slower to react to change. They seem to work best when directed to achieve focused objectives over a finite lifetime. As stated previously, the IMEC model of providing “research for hire” appears to be an effective approach to solving advanced technology challenges in a collaborative, pre-competitive environment. It would seem that there is potential for much more synergy and sharing between the various consortia and government-funded entities. Some recent announcements indicate closer collaboration on dielectric programs for example, but the industry could get more leverage if a coordinating body were to help manage these resources for less redundancy and more leverage.

An example of research coordination in the U.S. that was favorably cited by respondents, is MARCO (Microelectronics Advanced Research Corporation), which is a not-for-profit research management organization that funds and operates a number of microelectronics, university-based research centers. MARCO is a wholly-owned, but separately managed, subsidiary of the SRC (Semiconductor Research Corporation), the university research arm of the SIA (Semiconductor Industry Association). The MARCO program is not only sponsored by the SIA, but also by the U.S. Government’s DARPA, as well as a few equipment and materials suppliers. MARCO’s Focus Center Research Program (FCRP) is funding research at five multi-university centers to address the longer-range problems facing the extension of CMOS and new approaches to device physics. This is an excellent program for furthering research into semiconductor device technology, but does not encompass the scope of research required to support the materials and equipment industries.

Much of today’s government technology funding goes towards

furthering the device industry’s technology roadmap. Although the equipment and materials industry is supporting the chip industry, their challenges are not always the same as those of their customers. The highly competitive nature of the equipment and materials market limits how much pre-competitive work can be performed. Governments with a strong strategic desire to participate in the semiconductor equipment and materials business should recognize these differences and fund early “seed” research programs that support these vital sectors. Possible funding areas include new approaches and improvements in factory automation, efficiency and productivity, which could in turn generate new R&D initiatives that would deliver substantial manufacturing cost improvements to device makers.

Governments can also actively support workforce development in the long-term through the stronger education of basic science disciplines in schools and universities.

### CONCLUSIONS

Going forward, a gap will emerge between the demand for R&D to keep up with Moore’s Law, and the available supply of R&D funds in the equipment and materials industry. By 2010, it is estimated that this gap will grow to as much as US\$9.3 billion out of a total demand for \$19.7 billion in R&D funding.

This demand for increased R&D funding can be met in several ways. The most obvious is to increase R&D spending, but business models for the equipment and materials suppliers will not support this until revenues and gross margins improve. Meanwhile, there are efficiencies that could be gained if there were more focus at a pre-competitive level on speeding technology selection decisions and eliminating redundant and wasteful research. One example is in the area of lithography.

Beyond immersion, there are three major candidates for next generation lithography—extreme ultra violet (EUV, using 13 nm wavelength light), electron beam direct write, and nano-imprint. Each approach has its champion, but they all are fraught with serious technology and economic challenges. These challenges are not just in the area of equipment and materials, but also in the repetitive costs of the mask tooling required for each new chip design. The R&D investments will be extremely high, but not all will yield returns. This would appear to be an area in need of pre-competitive cost/benefit analysis and research to narrow the choices and align resources to ensure the success of the most likely solution.

As discussions begin on the migration to the next wafer substrate (currently planned as 450 mm diameter silicon), suppliers cannot see the demand beyond a very small number of large customers, and cannot fund the R&D necessary to implement it. A 450 mm program could take as long as seven to eight years to bring to market and is likely to cost the equipment and materials industries well over \$20 billion. Most equipment company executives question this direction and agree that funding would need to come directly from the device makers who reap the benefits. However, they also agree that no activity should be started until all economic issues and technology alternatives

have been thoroughly investigated. It is widely believed that there are alternative ways to deliver productivity improvements to the device community without the need for blindly scaling up to the next increment in silicon wafer diameter.

Some external research is performed at universities and consortia, but in this extremely competitive industry concerns about IP (intellectual property) protection tend to restrain the use of this type of resource. A solution could be the establishment of more independent research labs run along the same “research for hire” lines as IMEC. The integration task to develop new equipment and materials into working production processes is growing rapidly with each technology node. There are limited resources available to perform integration and hence there could be a need for more shared testing and integration labs, which would need to be independently operated.

These have become global issues now that the electronics, semiconductor, equipment, materials and sub-systems industries are located on multiple continents and in multiple time zones. Up until the last decade, semiconductor manufacturing was primarily centered in the U.S. and Japan, but today, major device manufacturers are located globally with an increasing trend to migrate chip and electronic manufacturing to Asia, with China being the newest nation to embrace semiconductor manufacturing. This globalization has put pressure on the supply industries to market, sell and support their products worldwide. Support costs include sales and service, but support also represents a drain of up to 30 percent on R&D budgets for the supplier base.

While companies have made significant progress over recent years to speed their internal time-to-market on R&D programs, much of the external development between materials suppliers, equipment manufacturers and device makers remains a serial process. There is opportunity for increased collaboration and more concurrent development practices to speed-up the increasingly complex integration task.

Consolidation in the equipment and materials industry is inevitable as smaller companies struggle to apply their innovative technologies in this increasingly global marketplace. The sub-systems suppliers that in turn supply modules to capital equipment OEMs have an even more difficult set of challenges as price pressures and support demands increase. Going forward, there may be more customer funding for custom engineering tasks that previously were performed on speculation by the sub-systems companies.

Finally, during the survey interviews, it was observed that only a few companies thought about stimulation of innovation and creativity among R&D staff. There is a shortage in the U.S., Europe and Japan of new physics, chemistry and engineering graduates to stimulate thought and maintain incumbent leadership in the semiconductor equipment and materials markets. Complacency has led the industry to believe that aggressive technology progression is synonymous with creativity, but there is still plenty of room for “out-of-the-box” thinking.

## Recommendations

This paper has encompassed a wide range of topics that impact R&D in the semiconductor equipment and materials industry. There are three key communities being addressed—suppliers, customers and government—so the following recommendations are addressed to each respectively. However, the biggest impact will result from increased collaboration and more effective sharing of both the decision-making and the R&D efforts to keep the collective industry on “Moore’s Law.”

### The Supplier Base

The supplier base should continue to improve the current R&D funding paradigm through both efficiency improvements and growth. Approaches might include:

- **Seek more effective partnering and collaboration both vertically and horizontally to share R&D costs and risks, reducing time-to-market via concurrent development programs**
- **Obtain funding from customers or government bodies for longer-term research projects**
- **More actively leverage university research on basic technologies to stimulate “out-of-box” thinking**
- **Continually strengthen their business models for long-term sustainability in this cyclical and volatile market**
- **Participate actively in the ITRS and consortia to help drive faster roadmap decisions and avoid “blind alleys”**
- **Diversify where possible into new markets to leverage R&D**

### Customers

The device-maker customers should understand the R&D funding issues facing their supplier base and partner with them in long-term relationships to ensure a more efficient spending of scarce R&D funds for a win-win return on investment. This will ensure a stronger supplier base capable of sustaining future technology developments. Approaches might include:

- **Investing in, or funding suppliers that are needed to support higher-risk, longer-return projects, and help these suppliers achieve faster ROI**
- **Where possible, outsource process development and integration tasks to suppliers and consortia, where there can be more leverage on funds spent on R&D**
- **Enhancing the ITRS role by ensuring it’s grounded in economic as well as technological expertise, particularly to address the looming challenges of the next wafer substrate size and next generation lithography**
- **Encouraging more non-linear and “out-of-the-box” thinking versus simply charging at full speed along the established roadmap**

- More actively include suppliers in consortia and roadmap discussions to address issues as early as possible in the development process
- Support university research that is focused on supplier-related technologies that underlie semiconductor technology

### Governments

The semiconductor industry is vital to jobs, long-term economic health and national security. The various governments must essentially play a supportive and constructive role to encourage and nurture these industries that are at the heart of all technology-based economies. In this increasingly global market, industry will

move to locations where there are stronger factors supporting its growth. Approaches to address this might include:

- Providing financial and economic incentives to stimulate investments in R&D
- Directly funding basic science research for innovative solutions in long-term, high-risk areas
- Supporting the education of basic science disciplines through schools and universities to develop the workforce
- Stimulating the availability of early-stage venture funding for creative start-ups that address critical areas

## APPENDICES

### I. Industry Background

- Demand for ongoing R&D is relentless to keep Moore's Law on track
- Semiconductor industry cyclicalities continues despite slowing average growth rates
- Electronics commoditization has exerted intense price pressure on the food chain

### The Semiconductor Supply Chain

The semiconductor manufacturing industry is part of the larger electronics supply chain, consisting of electronic end equipment, semiconductors, semiconductor equipment, and materials. The key components in electronic products are semiconductor chips or integrated circuits, which enable electronic goods to be made more powerful, capable and cheaper every year. To manufacture these chips requires very sophisticated technology, constant research and development, as well as complex, expensive capital equipment and many ultra-pure materials.

The semiconductor manufacturing business has in aggregate grown enormously, but has experienced major boom-bust cycles over the years. Until the last decade, semiconductor manufacturing was primarily centered in the U.S. and Japan. Today, major device manufacturers are located in North America, Japan, South Korea, Taiwan, Southeast Asia, Europe and China. There is an increasing trend to migrate chip and electronic manufacturing to Asia, with China being the newest nation to embrace semiconductor manufacturing. This globalization has put pressures on the supply industries to market, sell and support their products worldwide.

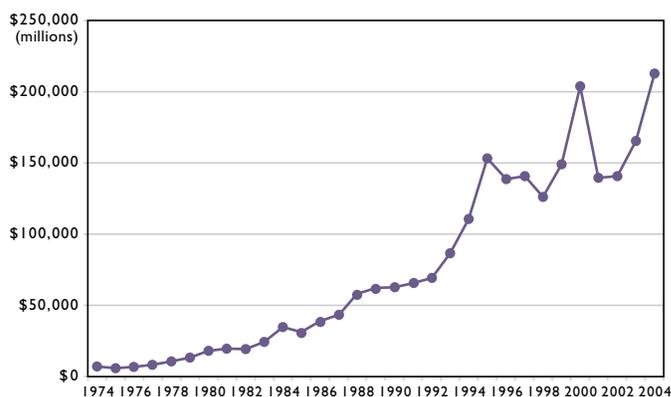
### Semiconductor Manufacturing Technology

Semiconductor technology constantly progresses at an extremely fast pace. This pace has been characterized by one of Intel's

co-founders, Gordon Moore. Over 30 years ago, Moore made the observation that the industry drives its technology forward to achieve a doubling of transistor density on integrated circuits every 18–24 months. This observation, known as "Moore's Law," describes the technologies that enable electronic chips to get smaller, better, faster and cheaper to deliver more electronic functionality into the hands of consumers. Transistors are the small components (like switches) that are combined on integrated circuits to make chips work—whether they be watches, calculators, computers, mobile phones, or any other electronic product.

The industry has quickly evolved from only being able to put a few tens of transistors on a chip in the late 1960s, to today when computer chips can contain hundreds of millions of transistors. What this has achieved, is to dramatically bring down the price of each transistor. The transistor function that cost \$1 each in 1968 now costs less than one ten-millionth of a dollar today! Today's state-of-the-art transistor is so small that conventional optical microscopes cannot even see it since it has dimensions that are less than one ten-millionth of a meter.

Global Semiconductor Sales



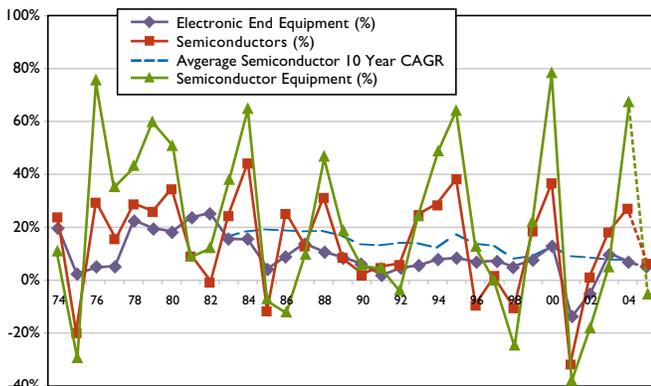
(Source: SIA)

This rapid technology development is what fulfills Moore's Law. However, it does not happen naturally. The industry's highly competitive and pioneering spirit has driven research and development at all levels, with funding coming from multiple sources. The primary source has been out of company gross profits, with some early-stage funding coming from the venture and equity markets, but this has scaled back in recent years. Government funding has occurred periodically for relatively small, focused research initiatives through various agencies.

**The Historical Business Cycles**

The semiconductor industry is characterized as "growth-cyclical." This is best seen by observing the following chart showing semiconductor revenues since 1974. It shows that, while the industry has experienced strong growth, it has not been smooth—but characterized by periods of forward surges followed by pull-backs. Clearly, the volatility of the last five years has been much more pronounced than in prior years. Another way to look at this is to examine the year-over-year growth rates.

**Electronics Growth Rates (year-over-year)**



(Sources: SIA, SEMI, Dept. of Commerce)

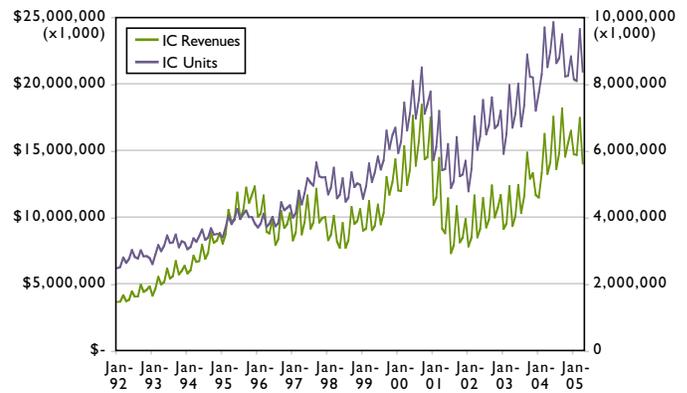
In the above (Electronics Growth) chart, the blue line (with diamond data points) shows the electronic end product sales growth which started out more volatile in the '70s, then began to stabilize around 7% as the industry matured in the 1990s. Note that it never experienced negative growth until 2001. The red line (with square data points) shows the more volatile semiconductor industry, swinging from +40% down to -20% and back again. The red dotted line is a rolling 10-year average of the growth, showing that the chip industry's average growth rate has slowed down from almost 20% in the '80s to almost 10% today. This is because the semiconductor/chip content in electronics products is saturating and growth is slowing. The next element of the "food chain" is the capital equipment segment (the green line with triangular data points), which is even more volatile than the chip industry. This is due to the surges in capital spending made in order to expand expensive manufacturing capacity—followed by weak periods after excess capacity was built.

**2001—The Worst Downturn Ever**

The most noticeable period in the above chart is the boom-bust

of the 2000–2001 period. It was the result of a combination of several unfortunate events, starting with the Y2K surge to build computer and network infrastructure prior to the millennium transition. On top of that came the infamous Dot.com bubble, which created much euphoria and excess spending on computer/communications infrastructure. The semiconductor industry had substantially over-built capacity during this period of strong demand. Then the bubble burst, and was closely followed by geo-political woes (terrorism, etc.). For the electronics industry in general and the semiconductor industry in particular, this was the worst downturn (recession) on record. In 2001, demand dropped for electronic goods and the chips that go into them. In recorded history, this was the first time that the electronics growth rate had gone into negative territory.

**Monthly IC Data**

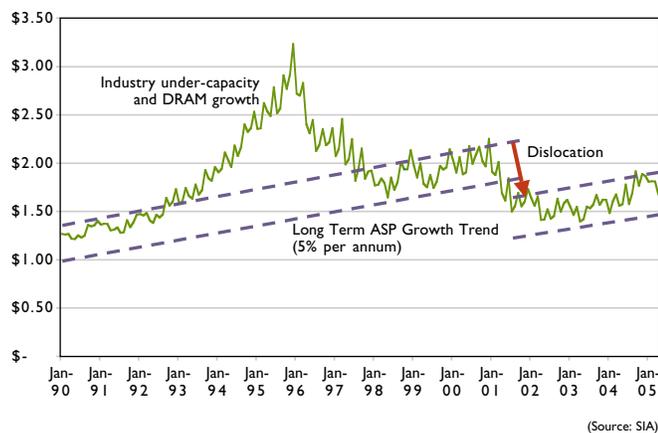


(Source: SIA)

One of the biggest impacts to the industry was the resulting price pressure. As with any commoditized product, pricing is a function of supply and demand. When there is insufficient supply to meet demand, prices remain high. When excess capacity comes on-stream, competitors fight over the available demand for their products and will drop the price to get the business in order to fill their factories. As the chart of monthly IC (integrated circuit) data shows, the IC units have recovered and are now running at almost 10 billion shipped per month—well ahead of the 8 billion per month peak of 2000. However, the chip revenues have only just managed to approach the \$18 billion per month peak of 2000. The reason for this discrepancy is the dramatic dislocation in pricing that has occurred since 2001.

This drop in pricing has put "the squeeze" on semiconductor companies and their entire supporting food chain. In 2001, with the bursting of the revenue "bubble," every company froze spending and hiring. Then, when the price cuts showed up in much reduced profit margins, the companies started cost cutting, layoffs, restructuring and project cuts. This reverberated all the way down the supply chain to equipment and materials companies. The previous chart shows how chip pricing dropped dramatically at the beginning of 2001 before reverting to the historical slow-growth trend line. This pricing dislocation is unlikely to ever be recovered, but its pain is shared across the industry.

### Chip Average Selling Price



Without the supply chain infrastructure of sophisticated equipment and materials, the semiconductor device makers would not be able to meet the continuing exponential demand for improved electronics price-performance. The semiconductor supply chain is a growth-cyclical industry that is starting to mature, and as a result is experiencing unprecedented change. In addition to technological change, the major changes include commoditization and globalization, which both bring tremendous opportunity for those who can quickly respond and adapt.

## II. Industry Financial Analysis

- All industry segments took a major hit during the 2001–2002 recession
- In real currency, only the semiconductor device industry has been able to substantially increase R&D spending
- Device manufacturers strengthened GM from 30% to 50% over the past 20 years
- Suppliers need to strengthen gross margins to expand R&D investments

This appendix will develop a baseline to quantify R&D spending and develop a picture to put it into perspective. This will be analyzed by looking first at the macro view of the semiconductor food chain, breaking it down into major components, then suggest ideal business models for long-term sustainable growth.

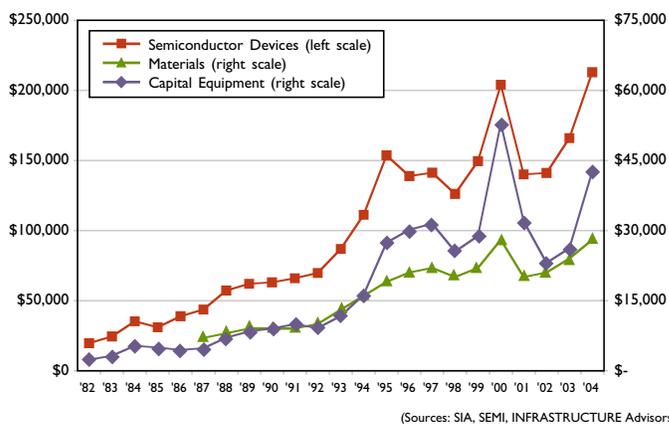
### The Macro View

Drawing from the Standard & Poor's financial database, an analysis was made of 54 companies that are publicly traded on the U.S. equities markets. Companies in other countries were examined, but the different accounting metrics and standards made it difficult to perform comparisons and aggregate the results in a meaningful way for the purposes of this study. Those selected were virtually pure-play in the semiconductor, capital equipment, sub-systems or materials sectors. Over the 20 years analyzed, not all companies were public throughout the period. However, for example, the equipment companies selected by 2000 represented well over 60% of worldwide industry revenues. There were seven major device makers selected representing over 35% of global semiconductor industry revenues. Since few mate-

rials companies are pure-play public entities, the eight selected only represented between 10% and 12% of materials industry revenues on a global basis.

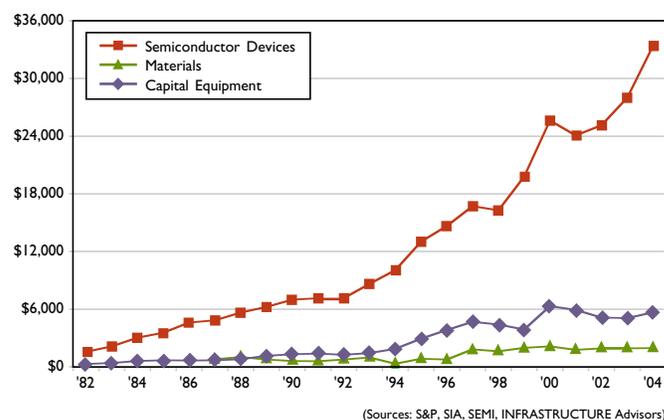
Over the last decade, semiconductor, semiconductor equipment and materials industry revenues have grown, but have become much more volatile. Since the 2000 semiconductor sales peak, chip sales have reached a new high, but the supplier base has not regained the prior peak levels.

### Industry Revenues (\$M)



By analyzing financial results of the target companies and extrapolating the results to the industry, we can see in the following chart a close estimation of the actual spending on R&D by these three sectors. The device maker R&D spending is accelerating as progress is made to each successive node along Moore's Law. Equipment and materials spending has flattened over the last five years and in subsequent charts, we will discover why.

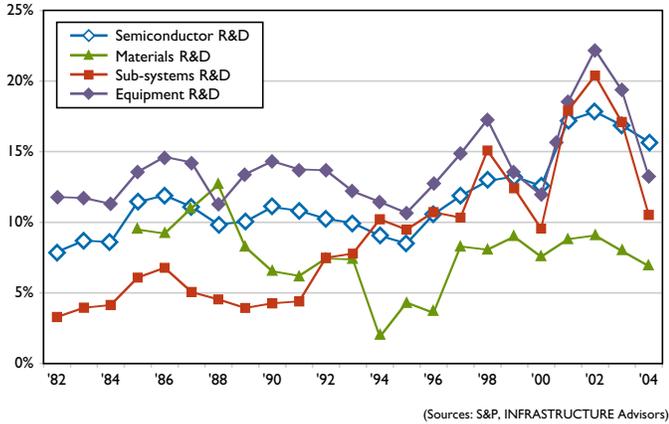
### R&D Spending (\$M)



Looking at the R&D spending expressed as a percentage of revenues in this next chart, it can be seen how the semiconductor device makers have increased spending from around 10% to around 17% over the last decade. At this level, we were also able to include a breakdown for the sub-systems companies.

This increasing percentage commitment, on top of semiconductor revenue growth, has enabled the significantly increased spending in real currency terms. These reported R&D figures for

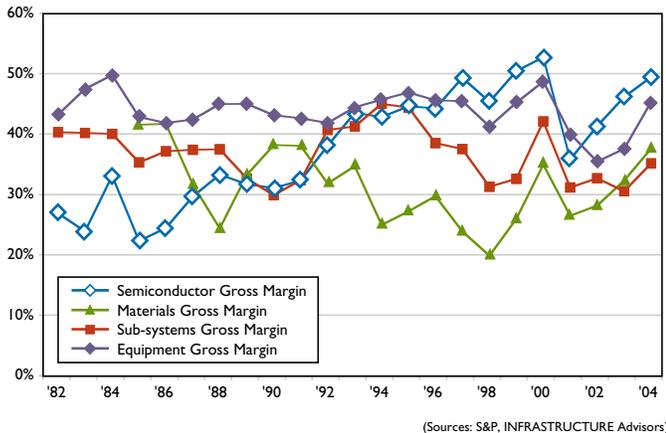
**R&D Spending (%)**



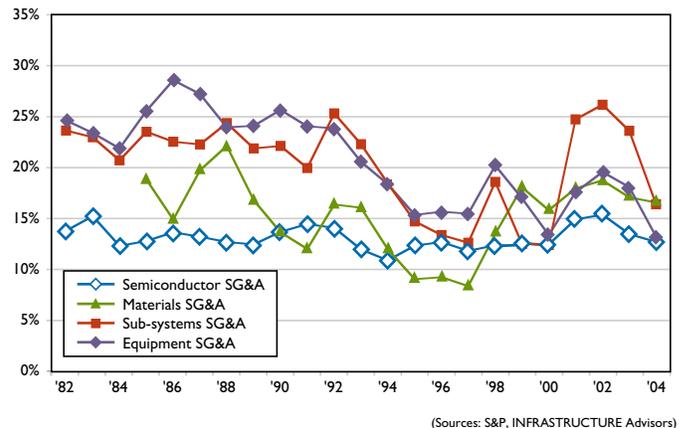
the chipmaker industry apply for spending on both process and product (design) R&D. It is relevant to look at both R&D elements since both are being driven upwards as the industry progresses down to smaller technology nodes on Moore's Law. The scope of this project did not include quantifying the device makers' R&D spending on process versus products; however, experience would place process R&D spending in the range of 15% to 20% of the total. The processes are becoming more complex and costly to develop/integrate into full-scale production. This complexity is also slowing the design process, raising the cost of product development and driving up the cost of mask tooling for the products.

During the same time period, capital equipment manufacturers have slightly elevated their spending as a percentage from an average 12.5% to over 15%; but, unlike the device makers, this has not been assisted by a base revenue growth. In fact, since 2000, the equipment manufacturers have managed to maintain actual spending levels in real terms and let the percentage run up to 20%. This is clearly not sustainable. The strong revenue growth of 2004 has once again helped bring down the R&D spending percentage, but it is unlikely that this will sustain throughout 2005. The 2004 revenue surge has brought the equipment R&D spending percentage substantially below that of the semiconductor industry for the first time.

**Gross Margin**



**SG&A Expenses**



Other than two excursions (upwards in the late '80s and downwards in the mid '90s), the material industry R&D spending has been maintained in the 7% to 9% range.

The sub-system segment has been taking on a steadily increasing share of R&D with spending going up from only 5% in the '80s to a current average around 15%. While the absolute spending is much less than other segments, the business model burden for this community is substantial.

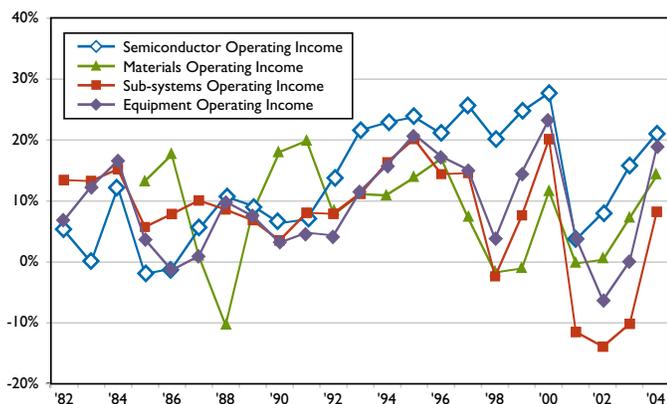
To understand how this increased semiconductor R&D spending has been funded, we need to look at gross margins for the answers. The semiconductor device industry has managed to drive gross margins up substantially over the last two decades from below 30% to the 50% range. This has primarily been enabled by "Moore's Law," with not all gains in cost reduction being passed on to end-customers via lower pricing. Some of these gains have been directed into building the business models to fund the ongoing progress of semiconductor technology.

For the equipment and sub-systems industries, the gross margins have fluctuated somewhat, but have not generally increased over that same time period. The materials industry suffered a "sag" in gross margins in the late '90s, but has been improving more recently as more high-value materials have been added into the process. For these suppliers, any increase in R&D has had to essentially come out of other areas such as SG&A (sales, general and administrative) expenses or profits.

Looking at the chart below, we see that the equipment and sub-systems industries both managed to bring down SG&A spending from the 25% of sales range to the high-teen range by 2000. Since that period, both have risen, with the sub-systems businesses having risen most. It would appear that much of this is due to the increasing demand for global support in the face of the industry recession post-2000. Similarly, the materials industry brought down SG&A percentages, but gave it all back in the last four years as support demands on new materials have increased. The semiconductor device makers have managed to hold a relatively steady 12% to 15% spending on SG&A over the entire two decades analyzed.

Operating Income is usually the “subtract answer” after R&D, SG&A and any miscellaneous spending is taken out of Gross Margin. For the early part of the '90s, all segments were running at profitable levels. The 1998 downturn caused a minimal hit to the chipmakers, but removed profitability from all other segments. The 2001 recession hit every sector's profitability, with the smaller sub-system industry being hit hardest.

### Operating Income



(Sources: S&P, INFRASTRUCTURE Advisors)

This historical analysis shows how the business models have changed and have come under pressure over time, with substantial impact being felt since 2000. The recovery of 2004 will be unlikely to extend into 2005, which is forecasted for the device makers to see only a slight increase in revenues. The materials industry, driven by a healthy chip unit demand should also see a small revenue increase, but the equipment and sub-systems industries are forecasted to see a reduction in revenues in 2005. R&D spending in real terms will likely be maintained, and will thus rise in percentage terms.

Clearly, all participants in this food chain must achieve healthy business models to survive and prosper in the long run. During periods of strong demand and growth, all participants fare well. However, this industry is very volatile and downturns take a very heavy toll in the revenues of the supplier industry segments. This causes extreme stress to business models and with these companies constantly striving to maintain R&D progress and global support; the result is frequent losses during downturns.

### Ideal Target Business Models

Most companies strive constantly to achieve their ideal “target” business models. However few, and usually only the larger com-

panies, manage to achieve these goals. The ultimate objective is the “bottom line,” or operating margin. This is the result of subtracting expenses from revenues, so the primary objective is to maximize revenues while minimizing costs. This is what everyone learns while in school, but achieving it in practice can often be quite a challenge. Not all expenses should be minimized, however. In particular, that includes R&D spending in high technology companies. To stay “in the game,” high-tech companies must constantly invest in the future. This means that they must have “deep enough pockets” to be able to maintain R&D spending in real terms through downturns, while avoiding losses at the bottom line.

In a cyclical industry like this, it is virtually impossible to maintain a static business model. However, the top companies maintain best-case and worst-case models for the peak and trough of the cycle respectively. Looking at the chart in the previous section, it is clear that the device maker community made a conscious effort to strengthen business models towards greater gross margins that could enable higher R&D investments while maintaining operating profits. The equipment, material and sub-system companies must do the same.

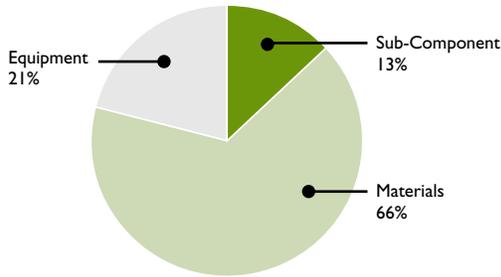
The following table shows, for each of the three industry segments, how the latest 2004 average business models compare to what we suggest as ideal ranges. The “min.” model represents the conditions when the industry is at a cycle trough and “max.” when it is at a cycle peak. The business should be structured to never lose money in downturns, and then enjoy profitability in the upturns.

The intent should be to fund R&D at a level to ensure future growth, and then essentially hold that level through downturns, letting the R&D percent of revenue rise as profitability and gross margins drop. To a lesser extent, the SG&A percentage should also rise in downturns, as customer support must be maintained. Naturally, to achieve this, the cost of goods must be minimized, as must any expense, but also revenues (pricing) must be maximized. In a highly competitive market it is not just pricing that is the “swing vote” in a procurement decision. Competitive situations in these segments are usually won primarily on the value of features and benefits. Competitive pricing pressures are often applied after the technical selection has been made in order to bring down the price on the selected product.

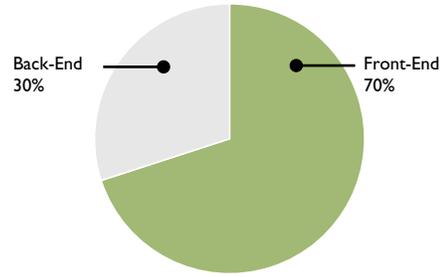
For the suppliers to further increase R&D spending, it will be necessary for them to strengthen gross margins. This will need to be a combination of cost reduction and more “value selling”

	Equipment Companies			Materials Companies			Sub-System Companies		
	Actual '04 Model	Ideal “Min.”	Ideal “Max.”	Actual '04 Model	Ideal “Min.”	Ideal “Max.”	Actual '04 Model	Ideal “Min.”	Ideal “Max.”
<b>Revenues</b>	100%	100%	100%	100%	100%	100%	100%	100%	100%
<b>Gross Margin</b>	45%	45%	50%	38%	35%	42%	35%	45%	45%
<b>R&amp;D</b>	14%	20%	15%	7%	10%	8%	10%	20%	10%
<b>SG&amp;A</b>	14%	20%	15%	17%	20%	14%	16%	20%	15%
<b>Operating Margin</b>	17%	5%	20%	14%	5%	20%	9%	5%	20%

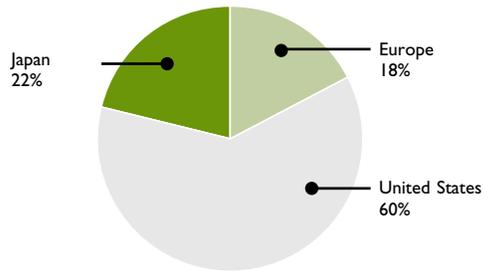
**Companies Interviewed—Segment Breakdown**



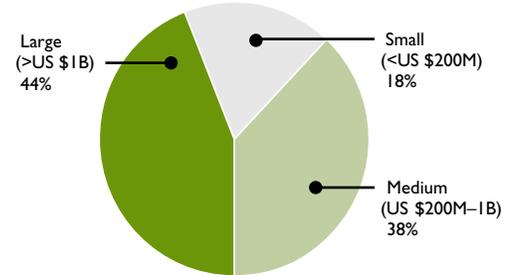
**Companies Interviewed—Sector Analysis**



**Companies Interviewed—Geographic Split**



**Companies Interviewed—By Size**



(Source: INFRASTRUCTURE Advisors)

to increase revenues. These objectives should be achievable as the industries mature and continue to grow.

**III. Survey Results**

- Interviews conducted across a wide representative sample of segments, sizes and demographics

In order to research the topic of R&D affordability for this paper, a survey was designed and used as the basis for discussions during interviews with 62 executives from 45 companies. The following four charts show the breakdown of the interviews by segment, sector, size and geography. As shown, this survey covered a wide representative sample of the industry.

The survey consisted of a few quantitative questions to help assess the spending profiles on R&D, but mainly comprised several open-ended qualitative questions to research the topic and stimulate discussion. In the following sections, the quantitative findings are summarized by segment, with the qualitative insight being summarized in the key topic sections of the main paper:

**R&D Spending**

During the survey, the participants were asked how their R&D spending split down into three broad categories. One category was “Research,” which is primarily the study or investigation to solve technology challenges. Another was “Development,” which is applying these results with expertise to create new products and take them to market. The third category was “Support,” which we shall discuss first before moving on to the other two categories.

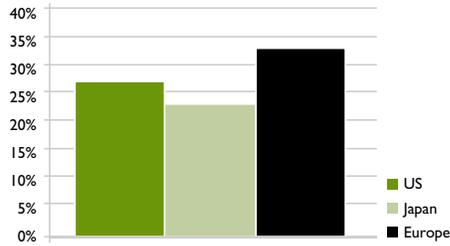
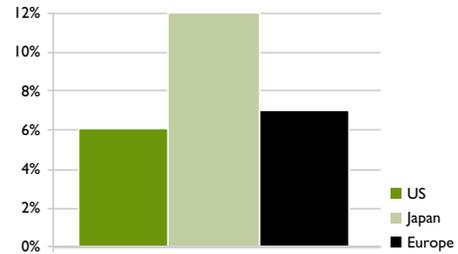
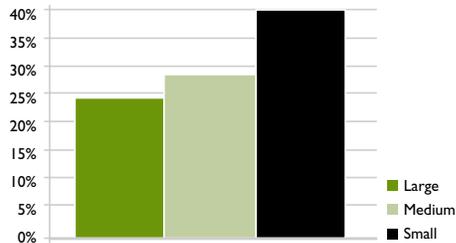
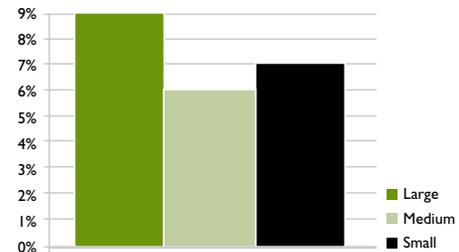
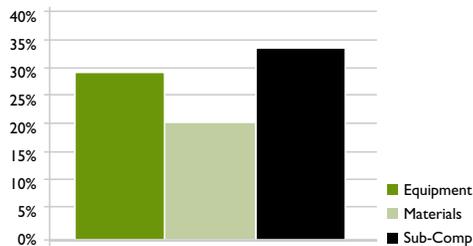
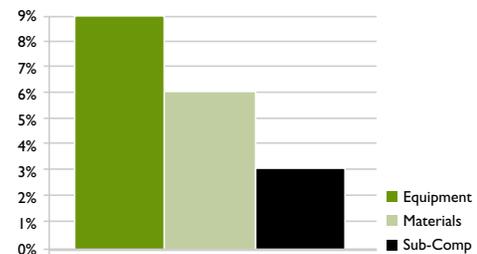
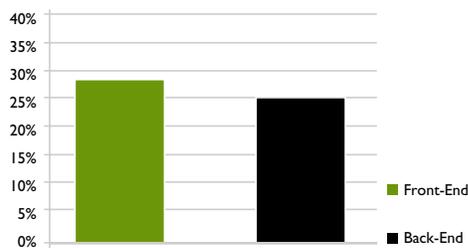
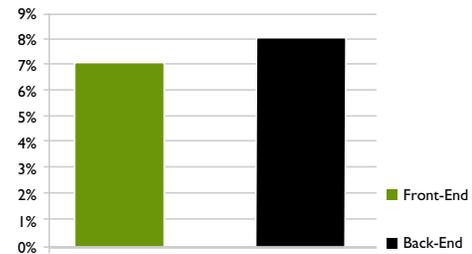
**R&D—Support**

When a new product is released to production, the job is seldom, if ever, “done” for the R&D staff. Despite thorough alpha and beta testing, customers find problems in the field, and manufacturing requires periodic support. R&D staff can find themselves flying to remote customer sites to help troubleshoot difficult on-site problems.

Customers also come back with requests for enhancements, additional feature changes and reliability improvements to improve tool performance. These are all valid requests, and are the right things to do in support of customers. Other than the obvious benefit of customer satisfaction, much can be learned for inclusion in the next generation of product to be developed. However, this all drains the “R&D Budget” from direct funding for new products.

Respondents were asked how much of their R&D budget is spent on this type of support, and the results are shown in the four charts to the right. We see that between 25% and 30% is spent on support, with an average across all segments of 28%.

Europe carries the largest support burden and Japan the lightest. It would appear that Europe’s smaller share of the device manufacturing business means that the equipment suppliers’ customers are more remote, causing higher support costs. In Japan, it seemed that most equipment companies had a more thorough set of product release procedures for better “out-of-box” quality, coupled with stronger manufacturing and support organizations.

**R&D % on Support by Demographic****R&D % on Research by Demographic****R&D % on Support by Company Size****R&D % on Research by Company Size****R&D % on Support by Supplier Type****R&D % on Research by Supplier Type****R&D % on Support by Fab or A/T Supplier****R&D % on Research by Fab or A/T Supplier**

(Source: INFRASTRUCTURE Advisors)

(Source: INFRASTRUCTURE Advisors)

Small companies clearly have heavier support costs due partly to the global support burden and also to the fact that their resources are not as “deep” as their larger counterparts. For certain skills, the really small companies may only have one or two experts to deploy.

In terms of segment, the materials companies have a much lighter support burden than the equipment companies due to the nature of the products. However, it is interesting to note the higher sub-component support burden, which is most likely caused by them serving two marketplaces—OEMs and device customers. There is little difference between front-end and back-end in this regard.

## R&D—Research

In general, the semiconductor capital equipment and materials industries spend a relatively small amount on pure “Research.” What is spent on it tends to be mainly applied research or feasibility studies targeted at the objective of developing and taking products to market as soon as possible.

Looking at the survey results demographically, we see that Japan spends almost twice the percent of sales on research as either the U.S. or Europe. Additionally, many of these Japanese companies are part of large multi-industry corporations with centralized extensive research labs. These central labs are available to the product groups to help solve pure research challenges and

it would appear that those costs are either in addition to the research numbers shown here, or are allocated corporate-wide, making Japan's investment ratio even higher in reality.

As expected, the larger companies have "deeper pockets," and can afford to spend almost 50 percent more on research than their medium and small counterparts.

The equipment companies report the highest R&D spending ratio on research, closely followed by the materials companies. The materials companies' numbers may be under-stated here since many are part of large conglomerates, who have corporate research labs that support the industry segment divisions with pure research.

Sub-component suppliers spend less since they are driven heavily by OEM customers to implement designs, with OEMs having completed much of the research. The main research is occurring at the automation and laser suppliers. There would not appear to be much difference between front and back-end.

**R&D—Development**

The lion's share of R&D spending goes towards the development costs involved in creating new products and bringing them to market.

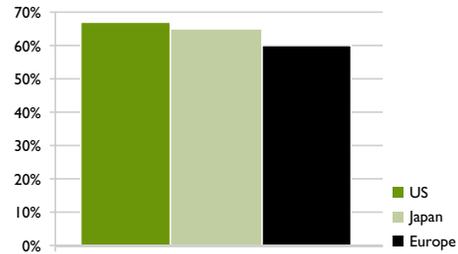
There are only slight variations demographically, by supplier type and by front-end/back-end. However, due to their heavy support costs, small companies do have noticeably less spending power available to support development activities.

For most companies the cost of developing a new product has remained relatively flat over time. Technology complexity has increased, but the management of R&D has become much more effective than in the past. Most companies now have regular management reviews where resource allocation decisions are made and projects are reviewed. Not only are projects reviewed for schedule, cost and performance, but they are also reviewed versus the roadmap and market dynamics to ensure that the demand still exists. Medium and larger companies are more effective in this regard.

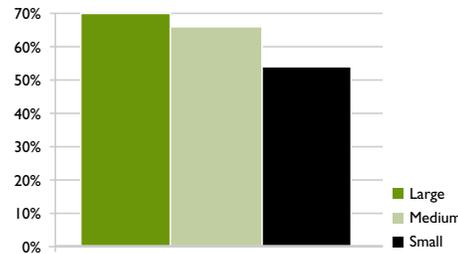
While the cost of developing a new tool has stayed relatively flat over time, the cost of integrating it into the process has risen dramatically with each technology node. At the 130 nm node and below, the equipment suppliers noticed a sharp increase in process complexity with more layers and new materials. This made the integration task much more difficult and time consuming—both in-house at the OEM during development, and at the customer sites. Any given process will typically have subtle differences at each customer site, requiring different integration activities to get the desired results. On average, front-end tool OEMs estimated a 20percent rise in the cost of combined development and integration per node, and this will likely increase below 90 nm.

Similarly, the development of new materials is increasing rapidly with each node—once again caused by the increasing integration costs.

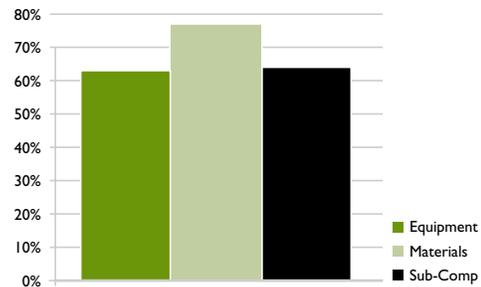
**R&D % on Development by Demographic**



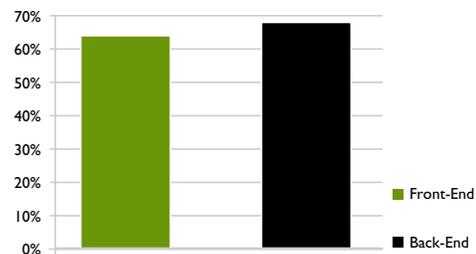
**R&D % on Development by Company Size**



**R&D % on Development by Supplier Type**



**R&D % on Development by Fab or A/T Supplier**



(Source: INFRASTRUCTURE Advisors)

#### IV. Participating Companies

Our appreciation goes to individuals, companies and organizations who gave time, information and insight to support the survey interviews, which were conducted to support this white paper. The following is a partial list of participants.

- Advanced Energy Industries, Inc.
- Advantest Corporation
- Agilent Technologies
- Air Products and Chemicals, Inc.
- Aixtron AG
- Applied Materials, Inc.
- ASET
- ASM Holding, N.V.
- ASM Pacific Technology, Ltd.
- Asyst Technologies, Inc.
- ATMI, Inc.
- Axcelis Technologies, Inc.
- Brooks Automation, Inc.
- Canon, Inc.
- Credence Systems Corporation
- Cymer, Inc.
- Dai Nippon Screen Mfg Co., Ltd
- Disco Corporation
- The Dow Chemical Company
- EKC Technology, Inc.
- Electro Scientific Industries, Inc.
- EV Group
- FSI International, Inc.
- Genus, Inc.
- Hitachi High-Technologies Corporation
- IMEC
- KLA Tencor Corporation
- Kulicke and Soffa Industries, Inc.
- LAM Research Corporation
- Mattson Technology, Inc.
- Micro Component Technology, Inc.
- Micronic Laser Systems
- Nikon Corporation
- Novellus Systems, Inc.
- Photronics, Inc.
- Sumco USA
- Silicon Manufacturers Group (SEMI)
- Tegal Corporation
- Teradyne, Inc.
- Tokyo Electron, Ltd.
- Toshiba Ceramics Co., Ltd.
- Unaxis Management AG
- Yokogawa

#### V. About the Author



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##### INFRASTRUCTURE Advisors

Providing Independent Research and Consulting Services to the Semiconductor, Equipment and Related Industries

Ron Leckie has over 35 years of experience in the semiconductor manufacturing industry. This includes 14 years of engineering and manufacturing within the semiconductor industry and 11 years in the capital equipment industry, where he led the development and marketing of state-of-the-art semiconductor test systems. Since 1995, he has been an analyst and consultant to the industry.

During his career in the semiconductor industry, Ron worked on logic, memory and analog chips in the roles of operations, yield management, quality/reliability, product and test engineering. In the equipment industry, he gained his marketing skills, managed a product P&L center to develop and bring new products

to market, and was a member of the Megatest Executive Staff, which took the company through a successful turn-around and IPO.

Ron has published numerous articles and papers, and has participated in many panel discussions on the business and technical aspects of the industry. He earned the Bachelor of Science Degree with Honours in Electrical & Electronic Engineering in 1970 from Heriot Watt University, Scotland.

Ron is currently President of INFRASTRUCTURE Advisors, an independent research and consulting practice. He is a member of the Boards of Directors of Wentworth Laboratories, Inc., and of Delphon Industries, LLC. He is also a board member of the Northern California British American Business Council and is a founding member of the GlobalScot Network. Ron is a very active volunteer on various SEMI committees.

#### VI. About SEMI

SEMI is a global industry association serving companies that develop equipment, materials and services used to manufacture semiconductors, displays, nano-scaled structures, micro-electromechanical systems (MEMS) and related technologies. SEMI maintains offices in Austin, Beijing, Brussels, Hsinchu, Moscow, San Jose (Calif.), Seoul, Shanghai, Singapore, Tokyo and Washington, D.C. For more information, visit [www.semi.org](http://www.semi.org).